UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,782	07/28/2003	Seiji Kaneko	81940.0052	5210

26021 7590 09/09/2005

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
FARROKH, HASHEM	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,782	KANEKO ET AL.	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8,10,11,13,15-18 and 21-24* is/are rejected.

7)☒ Claim(s) *7,9,12,14,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/28/03,9/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The instant application having application No. 10/628,782 has a total of 24 claims pending in the application; there are 4 independent claims and 20 dependent claims, all of which are ready for examination by the examiner. The Examiner also notes the Applicants' preliminary amendment of claim 1 and cancellation of claim 5.

INFORMATION CONCERNING IDS:

The information disclosure statements (IDSs) submitted on 7/28/03 and 9/17/04 have been considered by the Examiner. The submissions are in compliance with the provisions of 37 CFR 1.97.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

Claim14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

1. Claim 14 recites "A disk array device according to claim 14...". A claim cannot depend from itself. A correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 10, 15-18, and 21-24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,173,377 B1 to Yanai et al. (hereinafter Yanai).

1. In regard to claim 1, Yanai teaches:

"A disk array device **(e.g., see column 12, lines 26-27; Fig. 4)** comprising:

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see column 7, line 61; elements 26 and 54 in Fig. 1).** *The host adaptors 26 and 54 shown in Fig. 1 receive the input/output host requests through* input/output channels.

"a plurality of cache memories provided for the corresponding respective input/output channels **(e.g., elements 28 and 64 in Fig. 1)**, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 7, line 64; elements 28 and 64 in Fig. 1).**

"a disk drive device;" **(e.g., see column 12, lines 40-42; elements 223a-223d in Fig. 4).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 7, lines 63-66; elements 16 and 44 in Fig. 1).** *For example data transfer (e.g., I/O) between the host A and disk 20 is performed by the controller 16.*

"and at least one communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 7, lines 60-63; elements 26 and 54 in Fig. 1).** *For example channel adaptors 26 and 54 represent the* communication module recited in the claim.

"a control module that controls **(e.g., elements 16 in Fig. 1)**, upon receiving a data input/output request from the at least one external device **(e.g., see column 2, lines 60-67; element 12 in Fig. 1)**, an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories." **(e.g., see column 19, lines 57-60; column 23, line 19-20; column 24, lines 60-67).** *For example the host data is being written to the cache then is transferred to the disk. The data in primary and secondary caches are synchronized and consistency and state of data or volumes is maintained by flags.*

10. *In regard to claim 10, Yanai teaches:*

"A disk array device comprising:" **(e.g., see column 12, lines 26-27; Fig. 4).**

"a plurality of input/output channels that receive data input/output requests from at least one external device;" **(e.g., see column 7, line 61; elements 26 and 54 in Fig. 1).**

"a plurality of cache memories provided for the corresponding respective input/output channels **(e.g., elements 28 and 64 in Fig. 1)**, each of the cache memories connected to each of the corresponding respective input/output channels;" **(e.g., see column 7, line 64; elements 28 and 64 in Fig. 1).**

"a disk drive device;" **(e.g., see column 12, lines 40-42; elements 223a-223d in Fig. 4).**

"a disk control module that performs data input/output to and from the disk drive device;" **(e.g., see column 7, lines 63-66; elements 16 and 44 in Fig. 1).**

"a communication module that communicatively connects the input/output channels with the disk control module;" **(e.g., see column 7, lines 63-66; elements 16 and 44 in Fig. 1).**

"a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories;" **(e.g., see column 19, lines 57-60; column 23, line 19-20; column 24, lines 60-67).**

"and a control module that controls (**e.g., elements 16 in Fig. 1**), upon receiving a data input/output request from the at least one external device **(e.g., see column 2, lines 60-67; element 12 in Fig. 1)**, an execution order of a response processing to respond to the at least one external device according to the data input/output request and the consistency maintaining processing." **(e.g., see column 19, lines 57-60; column 23, line 19-20; column 24, lines 60-67).**

15. *In regard to claims 15 and 21, Yanai teaches:*

"wherein a plurality of logical volumes of logical storage regions is set on a storage region of the disk drive device **(e.g., see column 13, line 64)**, the data input/output request includes an identifier for identifying at least one of the logical volumes that is a

subject of the data input/output request, and further comprising a module that performs the control of the execution order according to the identifier included in the data input/output request." **(e.g., see column 16, lines 61-67; column 17, lines 1-13).**

16. *In regard to claims 16 and 22, Yanai teaches:*

"a module that connects to another disk array device;" **(e.g., see column 12, lines 50-52; element 246 in Fig. 4).**

"and a module that, upon receiving a data write request as the data input/output request **(e.g., see element 16 in Fig. 1)**, writes data designated by the data write request in the disk drive device **(e.g., see column 2, lines 62-65)**, and sends a write request for the data to the other disk array device." **(e.g., see column 5, lines 35-50).**

17. *In regard to claims 17 and 23, Yanai teaches:*

"wherein each of the input/output channels **(e.g., see elements 26 and 54 in Fig. 1)**, upon receiving a data write request **(e.g., see column 2, lines 62-65)**, operates in one of a write operation mode to write data in the disk drive device and a request send operation mode to send the write request to the other disk array **(e.g., see abstract)**, and further comprising a module that performs the control of the execution order depending on which one of the write operation mode and the request send operation mode one of the input/output channels that receives the data input/output request is operating in." **(e.g., see column 5, lines 35-50).**

18. *In regard to claim 18, Yanai teaches:*

"A method for controlling a disk array device," **(e.g., see column 12, lines 26-27; Fig. 4).**

"the disk array device comprising a plurality of input/output channels that receive data input/output requests from at least one external device," **(e.g., see column 7, line 61; elements 12, 26, and 54 in Fig. 1).**

"a plurality of cache memories provided for the corresponding respective input/output channels," **(e.g., elements 28 and 64 in Fig. 1).**

"each of the cache memories connected to each of the corresponding respective input/output channels," **(e.g., see column 7, line 64; elements 28 and 64 in Fig. 1).**

"a disk drive device," **(e.g., see column 12, lines 40-42; elements 223a-223d in Fig. 4).**

"a disk control module that performs data input/output to and from the disk drive device," **(e.g., see column 7, lines 63-66; elements 16 and 44 in Fig. 1).**

"a communication module that communicatively connects the input/output channels with the disk control module," **(e.g., see column 7, lines 63-66; elements 16 and 44 in Fig. 1).**

"and a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 19, lines 57-60; column 23, line 19-20; column 24, lines 60-67).**

"the controlling method comprising the steps of: receiving a data input/output request from the at least one external device;" **(e.g., see column 2, lines 60-67; element 12 in Fig. 1)**

"and controlling an execution order of a response processing to respond to the at least one external device according to the data input/output request and the consistency maintaining processing." **(e.g., see column 19, lines 57-60; column 23, line 19-20; column 24, lines 60-67).**

24. *In regard to claim 24, Yanai teaches:*

"A storage system comprising:" **(e.g., see column 1, lines 25-30; Fig. 1).**

"at least one external device;" **(e.g., see column 7, line 53; element 12 in Fig. 1)**

"and a disk array device including a plurality of input/output channels that receive data input/output requests from at least one external device," **(e.g., see column 7, line 61; elements 26 and 54 in Fig. 1).**

"a plurality of cache memories provided for the corresponding respective input/output channels," **(e.g., elements 28 and 64 in Fig. 1).**

"each of the cache memories connected to each of the corresponding respective input/output channels," **(e.g., see column 7, line 64; elements 28 and 64 in Fig. 1).**

"a disk drive device," **(e.g., see column 12, lines 40-42; elements 223a-223d in Fig. 4).**

"a disk control module that performs data input/output to and from the disk drive device," **(e.g., see column 7, lines 63-66; elements 16 and 44 in Fig. 1).**

"a communication module that communicatively connects the input/output channels with the disk control module," **(e.g., see column 7, lines 63-66; elements 16 and 44 in Fig. 1).**

"and a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," **(e.g., see column 19, lines 57-60; column 23, line 19-20; column 24, lines 60-67).**

"wherein the disk array device includes a control module that controls (**e.g., elements 16 in Fig. 1**), upon receiving a data input/output request from the at least one external device," **(e.g., see column 2, lines 60-67; element 12 in Fig. 1).**

"an execution order of a response processing to respond to the at least one external device according to the data input/output request and the consistency maintaining processing." **(e.g., see column 19, lines 57-60; column 23, line 19-20; column 24, lines 60-67).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 6, 8, 11, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Yanai in view of U.S. Patent No. 6,792,507 to Chiou et al. (hereinafter Chiou).*

2. *In regard to claim 2 Yanai teaches all limitation recited in claim 1 but does not expressly teach:* "a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories."

Chiou teaches: "a consistency maintaining module that performs a consistency maintaining processing to maintain consistency of data stored in each of the cache memories." **(e.g., see column 6, lines 34-37)** *for maintaining cache coherency or consistency in the network storage system.*

Disclosures by Yanai and Chiou are analogous because both reference the storage system with plurality of cache memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the storage system taught by Yanai to include cache coherency (e.g., consistency) method disclosed by Chiou.

The motivation for cache coherency (e.g., consistency) as shown in column 2, lines 50-53 of Chiou would have been to provide a high performance, efficient cache system and method for network storage.

Therefore, it would have been obvious to combine disclosures by Chiou with Yanai for benefit of cache coherency or consistency as specified in the claims.

3. *In regard to claim 3, Chiou further teaches:*

"wherein the consistency maintaining module performs the consistency maintaining processing depending on a content of the data input/output request." **(e.g., see column 3, lines 23-31; column 6, lines 34-37).**

4. *In regard to claim 4, Chiou further teaches:*

"wherein the consistency maintaining module performs the consistency maintaining processing first depending on a content of the data input/output request **(e.g., see column 3, lines 23-31)**, and then a response processing to the external device is executed." **(e.g., see column 4, lines 4-17).** *For example when a write input/output request detected, a message regarding the write request is broadcasted and all cache managers in the network decide maintains cache coherency depending upon the amount of data, a cache invalidation or a cache update would be performed.*

6. *In regard to claims 6 and 11, Yanai teaches all limitation recited in claims 1 and 10 but does not expressly teach:* "when data stored in one of the cache memories is updated, the consistency maintaining module invalidates data stored in at least another one of the cache memories."

Chiou teaches: "when data stored in one of the cache memories is updated **(e.g., see column 2, lines 24-25)**, the consistency maintaining module invalidates data stored in at least another one of the cache memories." **(e.g., see column 3, lines 28-31)** *for invalidating the caches on the network that are on the same access zone when the amount of data is above some threshold.*

Disclosures by Yanai and Chiou are analogous because both reference the storage system with plurality of cache memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the storage system taught by Yanai to include cache coherency (e.g., consistency) including cache invalidation method disclosed by Chiou.

The motivation for cache coherency (e.g., consistency) including cache invalidation *as shown in column 2, lines 50-53 of Chiou would have been to provide a high performance, efficient cache system and method for network storage.*

Therefore, it would have been obvious to combine disclosures by Chiou with Yanai for benefit of invalidating caches as specified in the claims.

8. *In regard to claims 8 and 13, Yanai teaches all limitation recited in claims 1 and 10 but does not expressly teach:* "when data stored in one of the cache memories is updated, the consistency maintaining module updates data stored in at least another one of the cache memories."

Chiou teaches: "when data stored in one of the cache memories is updated **(e.g., see column 2, lines 24-25)**, the consistency maintaining module updates data stored in at least another one of the cache memories." **(e.g., see column 3, lines 28-31)** *for updating the caches on the network that are on the same access zone when the amount of data is below some threshold.*

Disclosures by Yanai and Chiou are analogous because both reference the storage system with plurality of cache memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the storage system taught by Yanai to include cache coherency (e.g., consistency) including cache updating method disclosed by Chiou.

The motivation for cache coherency (e.g., consistency) including cache updating as shown in column 2, lines 50-53 of Chiou would have been to provide a high performance, efficient cache system and method for network storage.

Therefore, it would have been obvious to combine disclosures by Chiou with Yanai for benefit of updating caches as specified in the claims.

ALLOWABLE SUBJECT MATTER

Claims 7, 9, 12, 14, 19 and 20 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

1. The primary reason for allowance of claims 7, 9, 12, 14, 19 and 20 in instant application is the combination with the inclusion of the following limitations: **wherein the data stored in the one of the cache memories and the data stored in the at least another one of the cache memories are stored in an identical storage region of the disk drive device.**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the***

title of the invention *such that it is descriptive of the invention as claimed as required be sec.* ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract*** *should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of* ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent Publication No. 2004/0078517 A1 to Kaneko et al. describes Disk array device, method for controlling the disk array device and storage system.

2. U. S. Patent No. 6,912,669 B2 to Hauck et al. describes Method and apparatus for maintaining cache coherency in a storage system.

3. U. S. Patent Publication No. 6,073,218 to DeKoning et al. describes Methods and apparatus for coordinating shared multiple raid controller access to common storage devices.

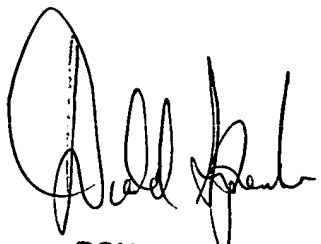
Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from **8:00 AM to 5:00 PM.**

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

2005-08-30



DONALD SPARKS
SUPERVISORY PATENT EXAMINER